

MAZE 16

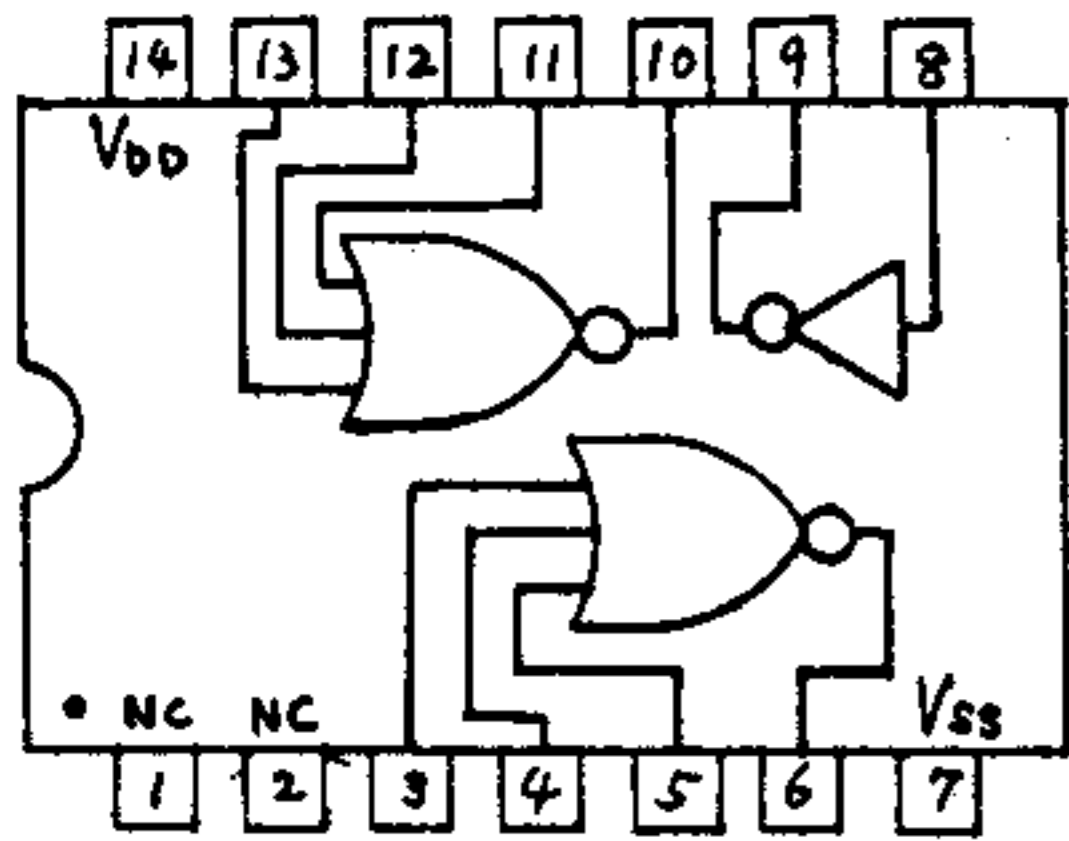
ikkei electronics のピン接続図

No. _____

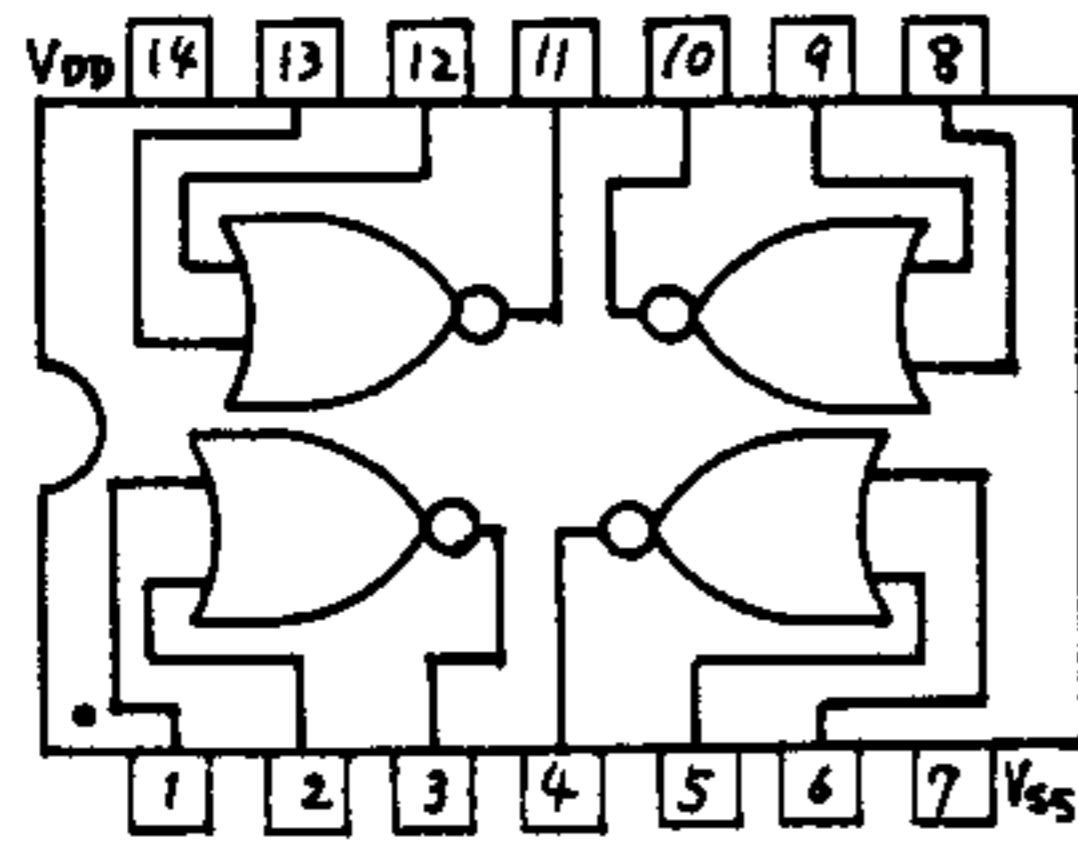
今回は、C-MOSのピン接続図のみです。特に、ゲート回路は「かり取り上げ」してみました。希望があれば、MSIや、TTLなどもやってみようかと思っています。

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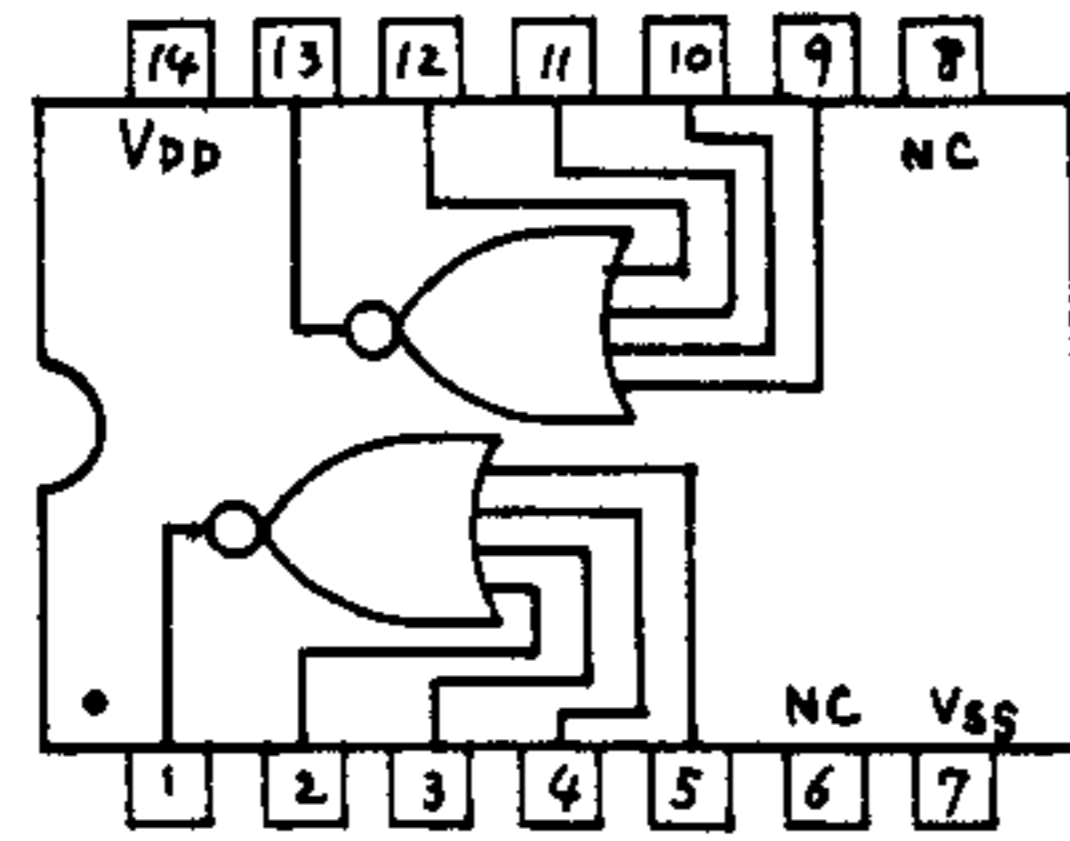
御意見御希望をお待ちしています。



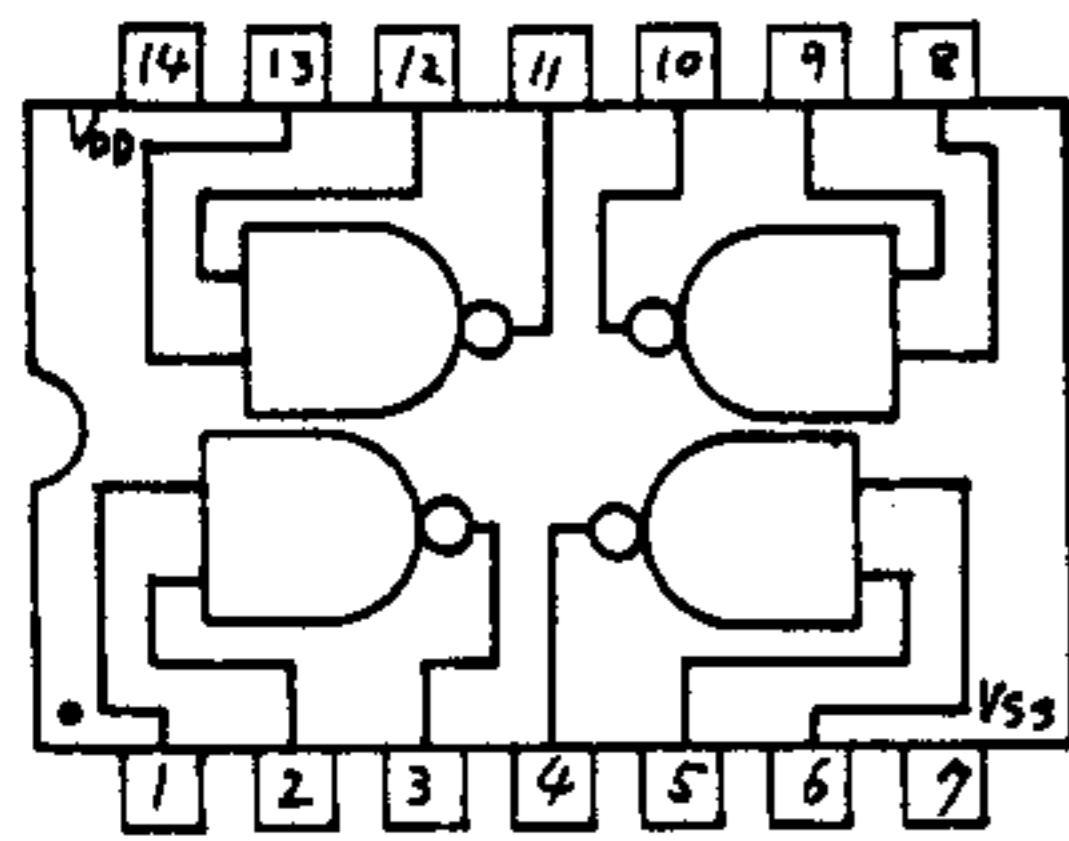
4000



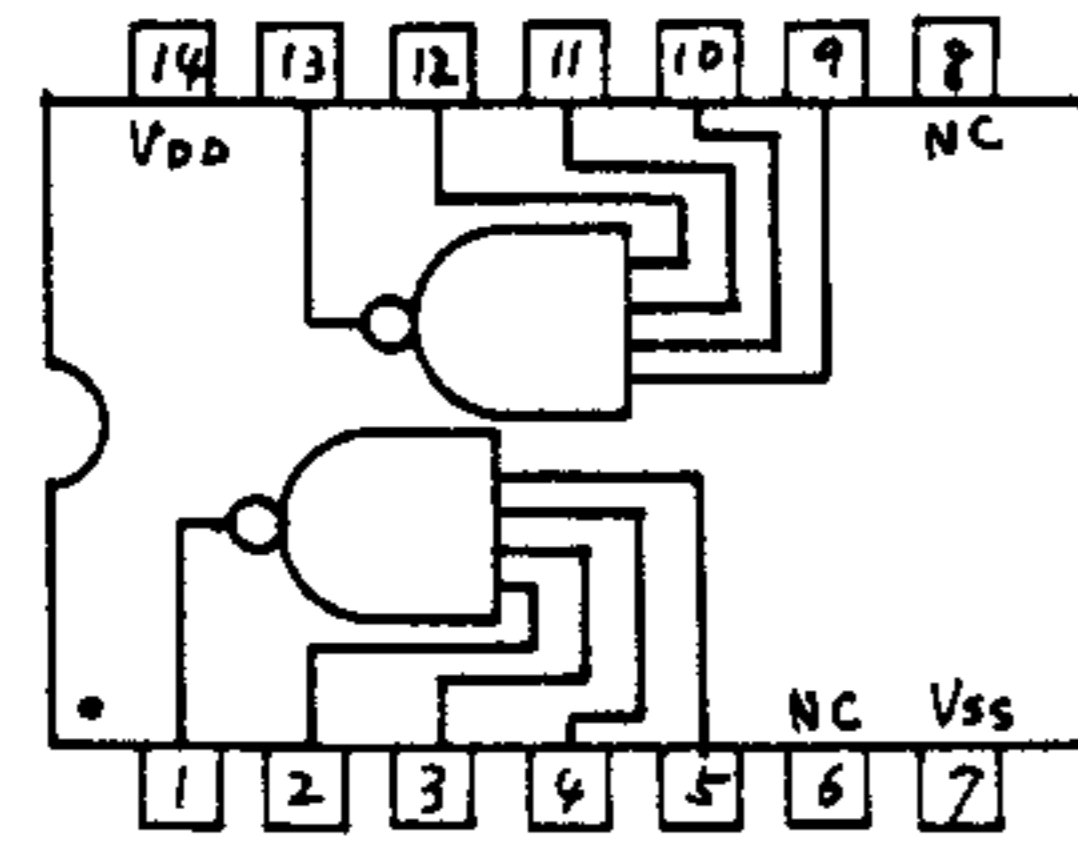
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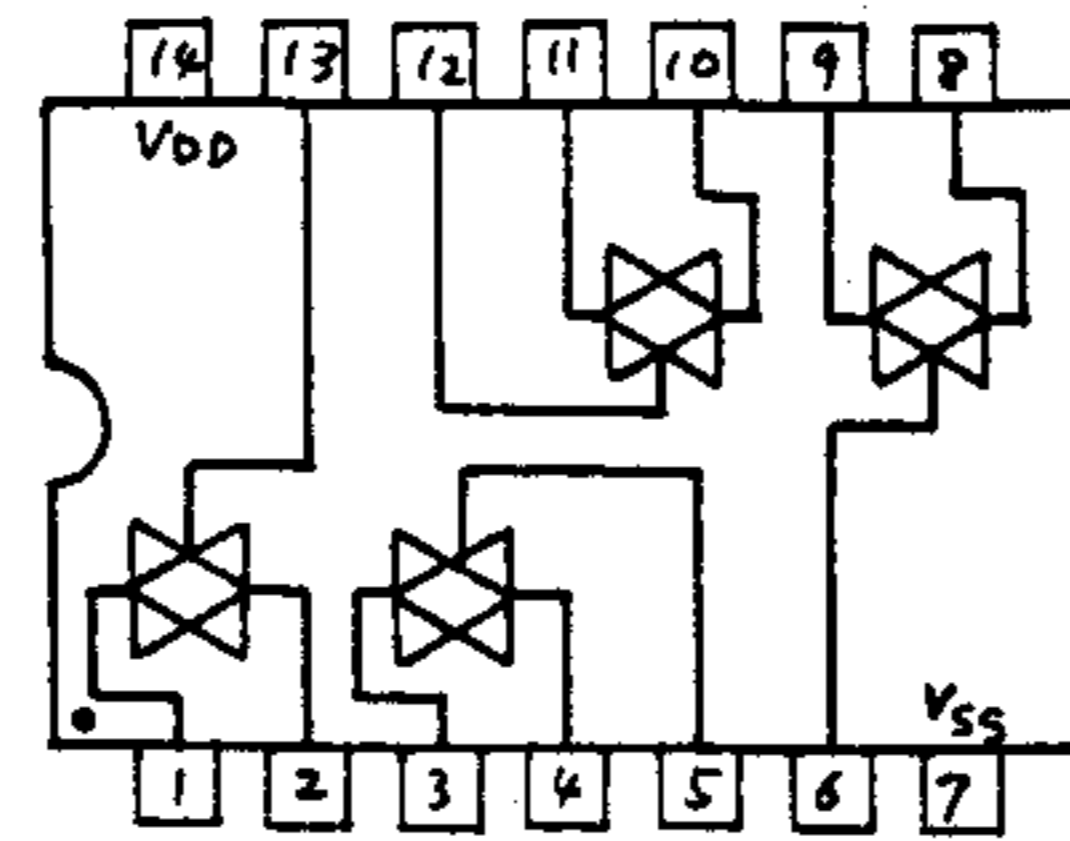
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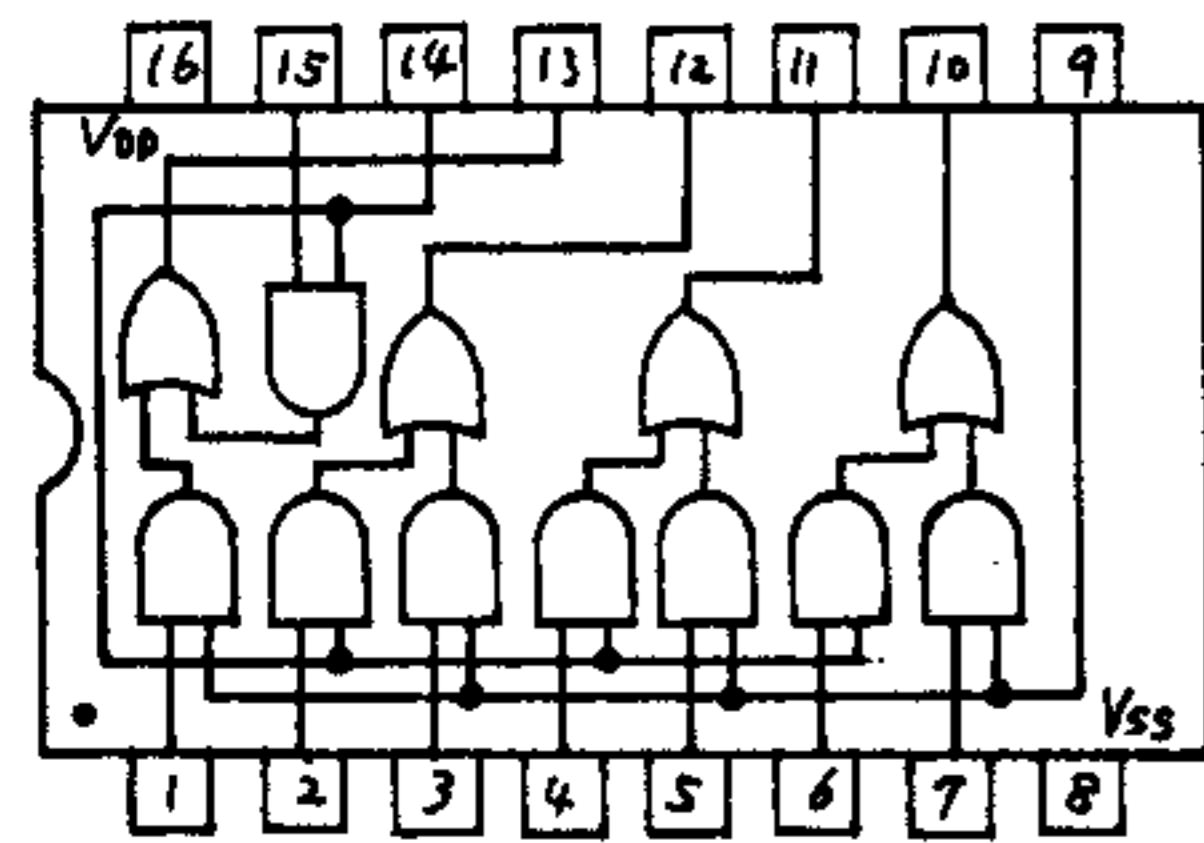
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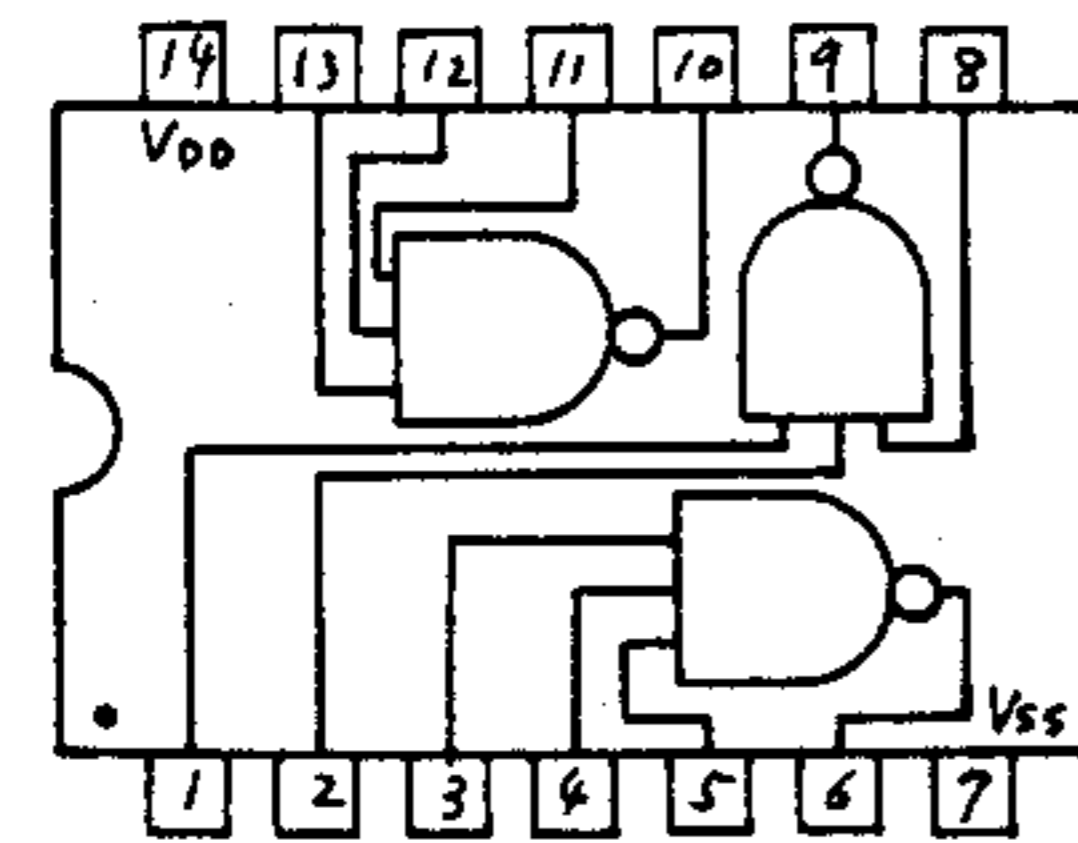
4012



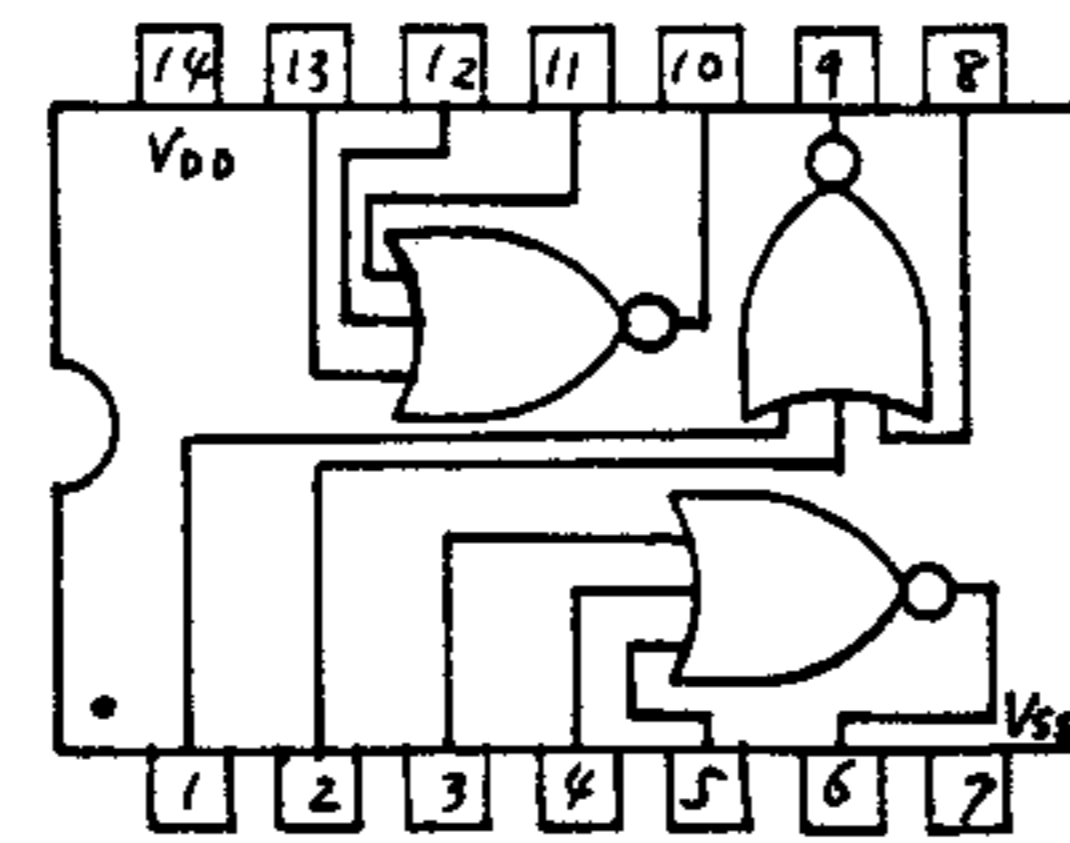
4066, 4016 4066は、4016を改良したもの
1: ON, 0: OFF



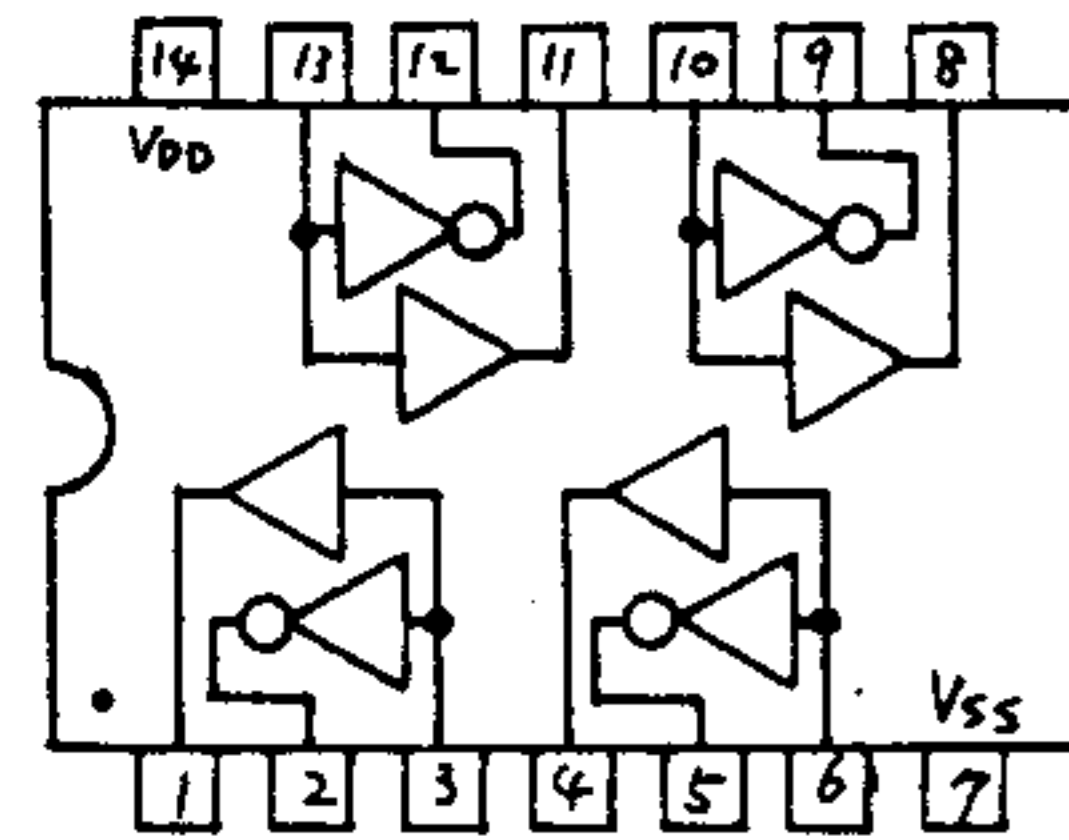
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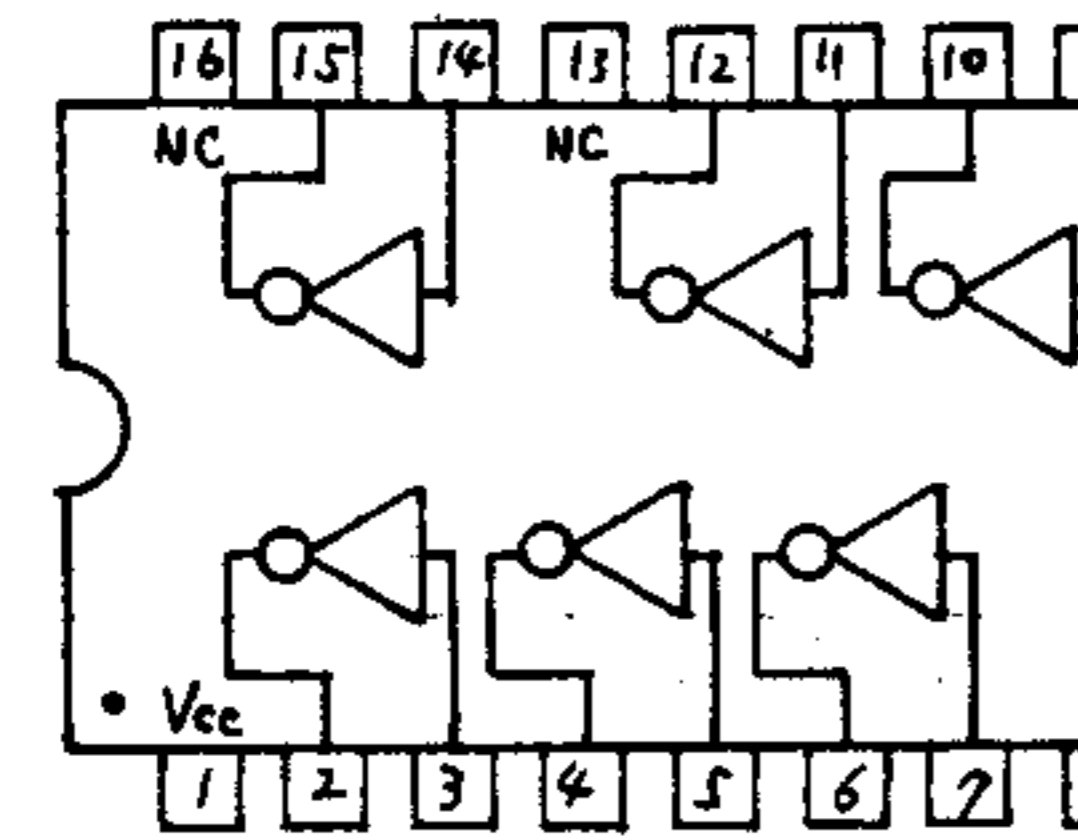
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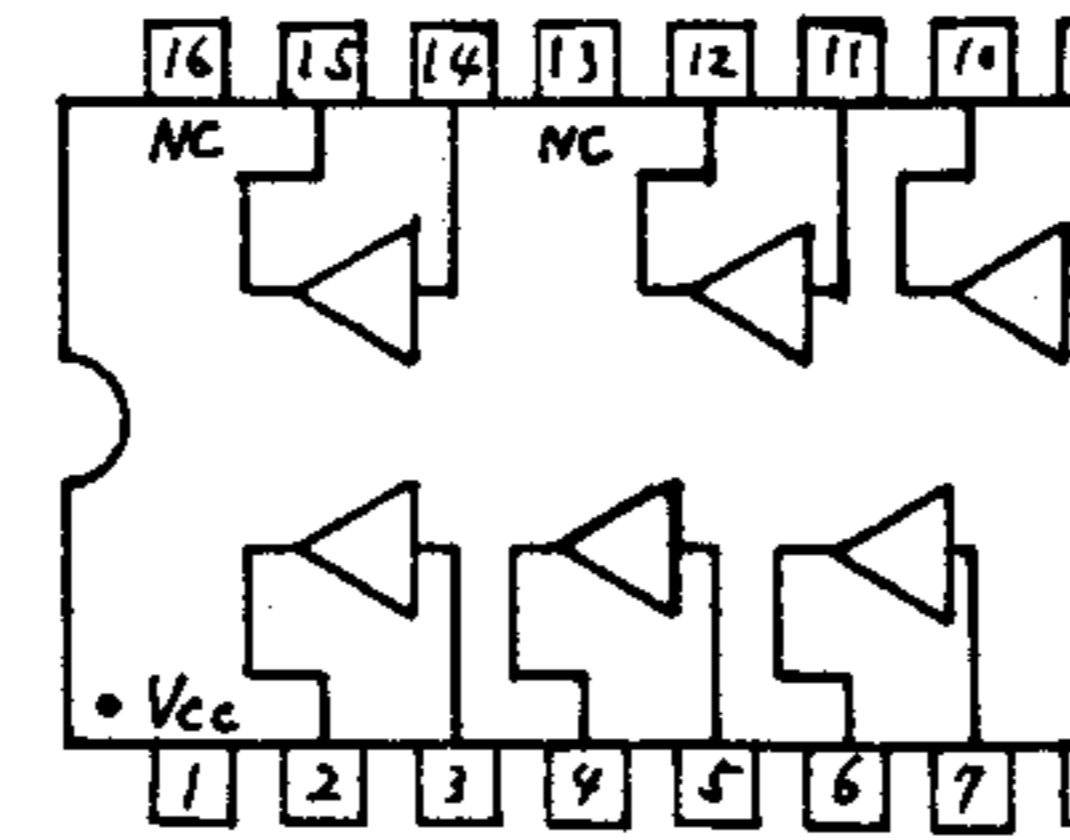
4025



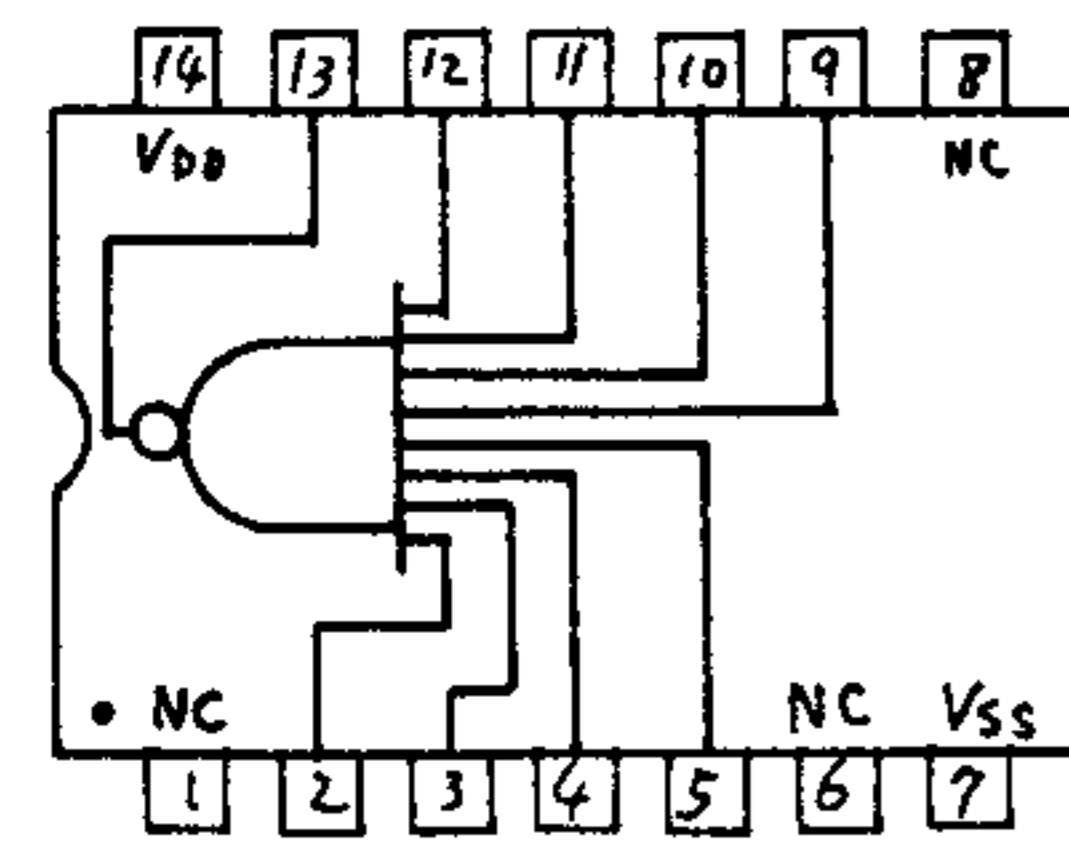
4041 BUFFER



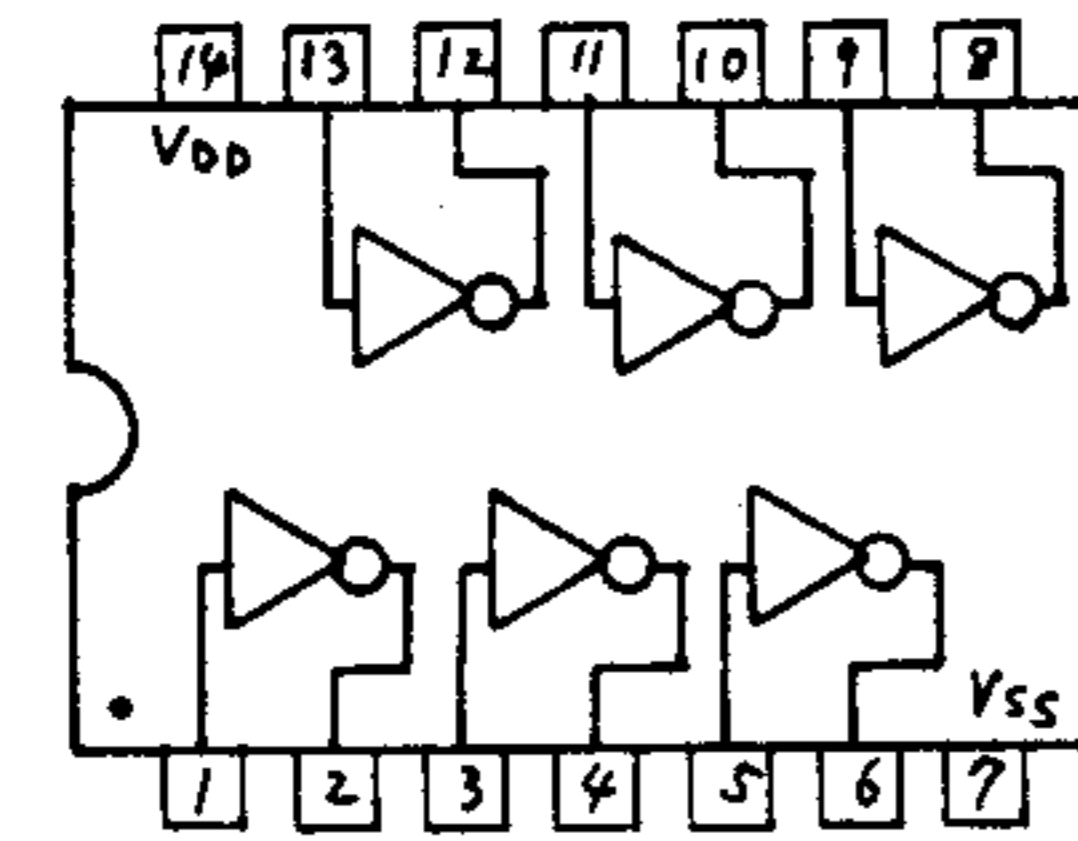
4049 BUFF $F_0 = 2TTL$



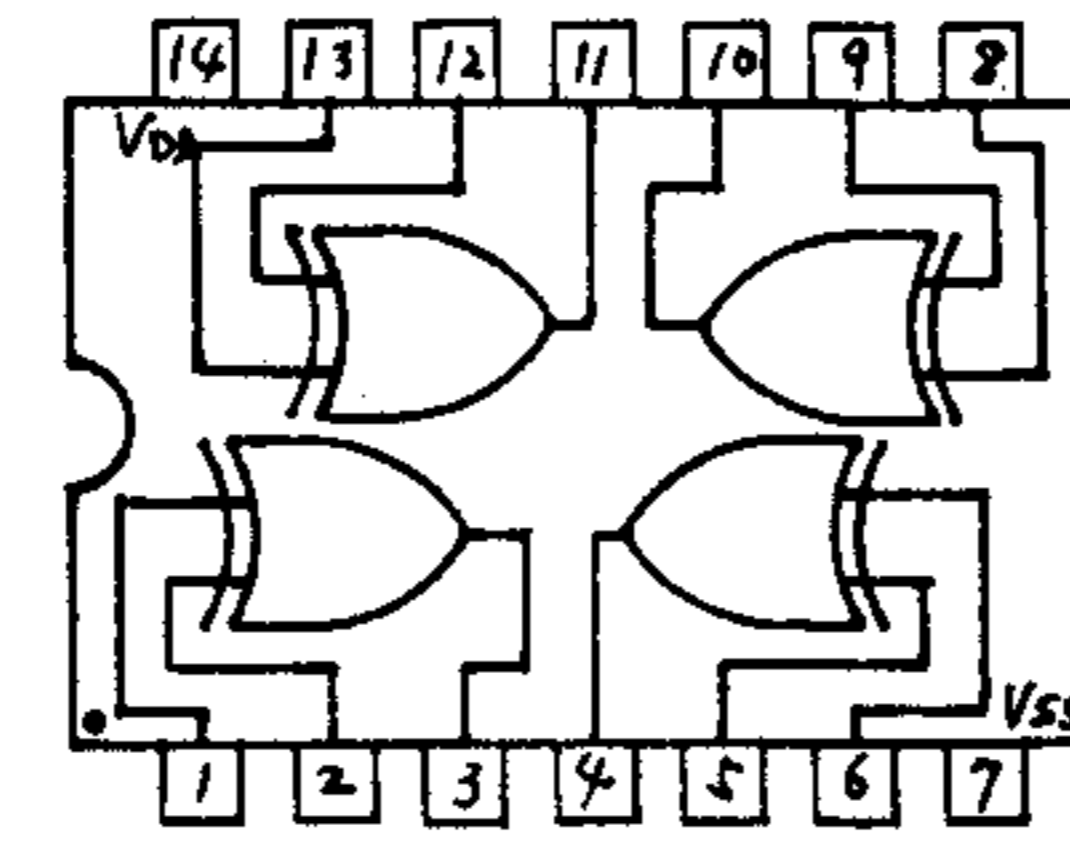
4050 BUFF $F_0 = 2TTL$



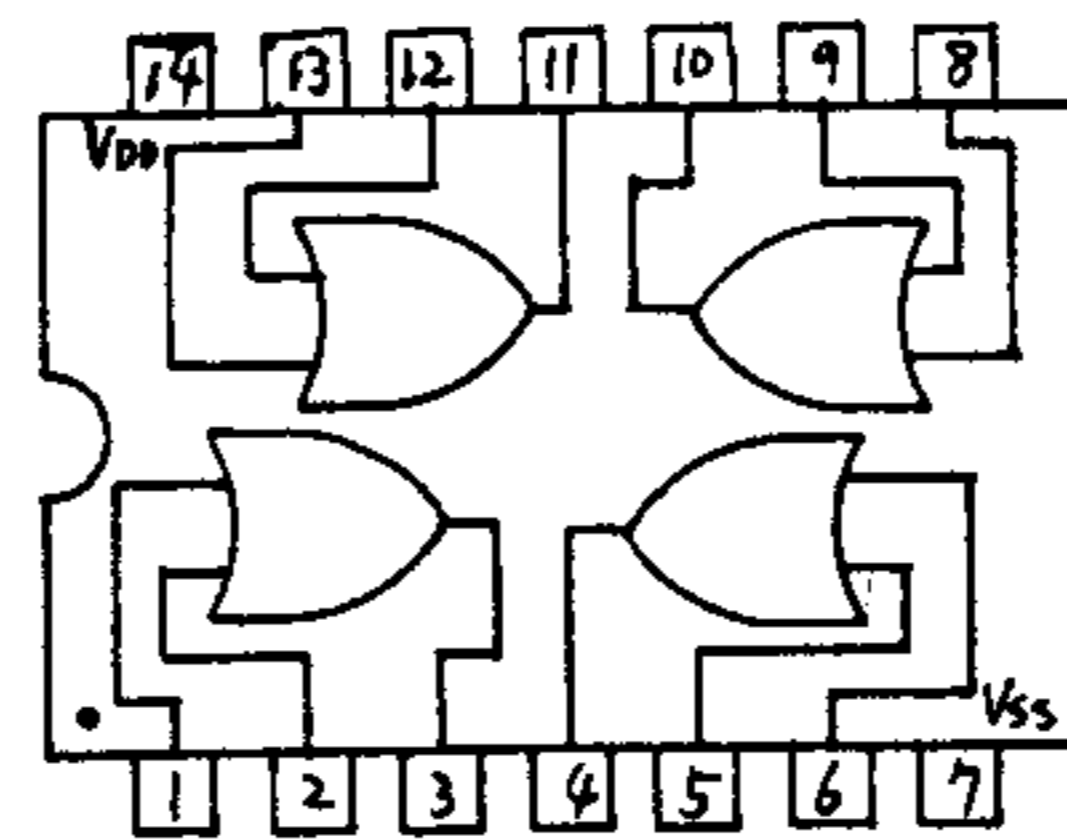
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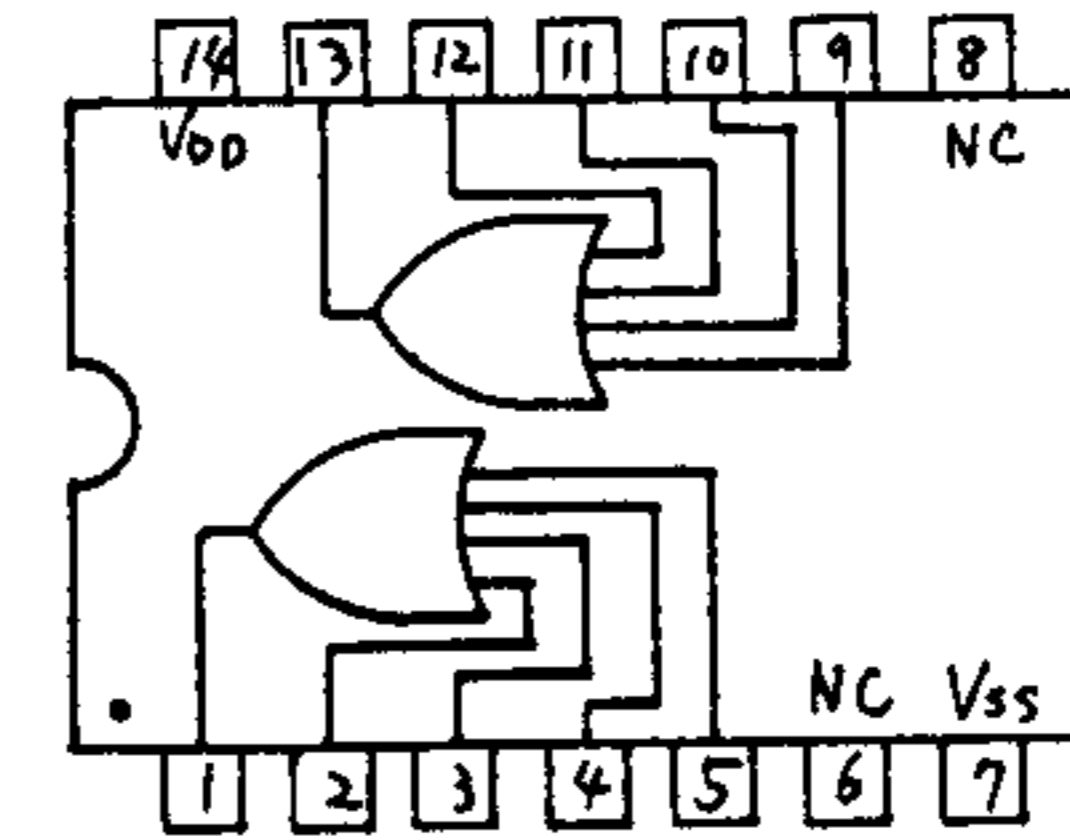
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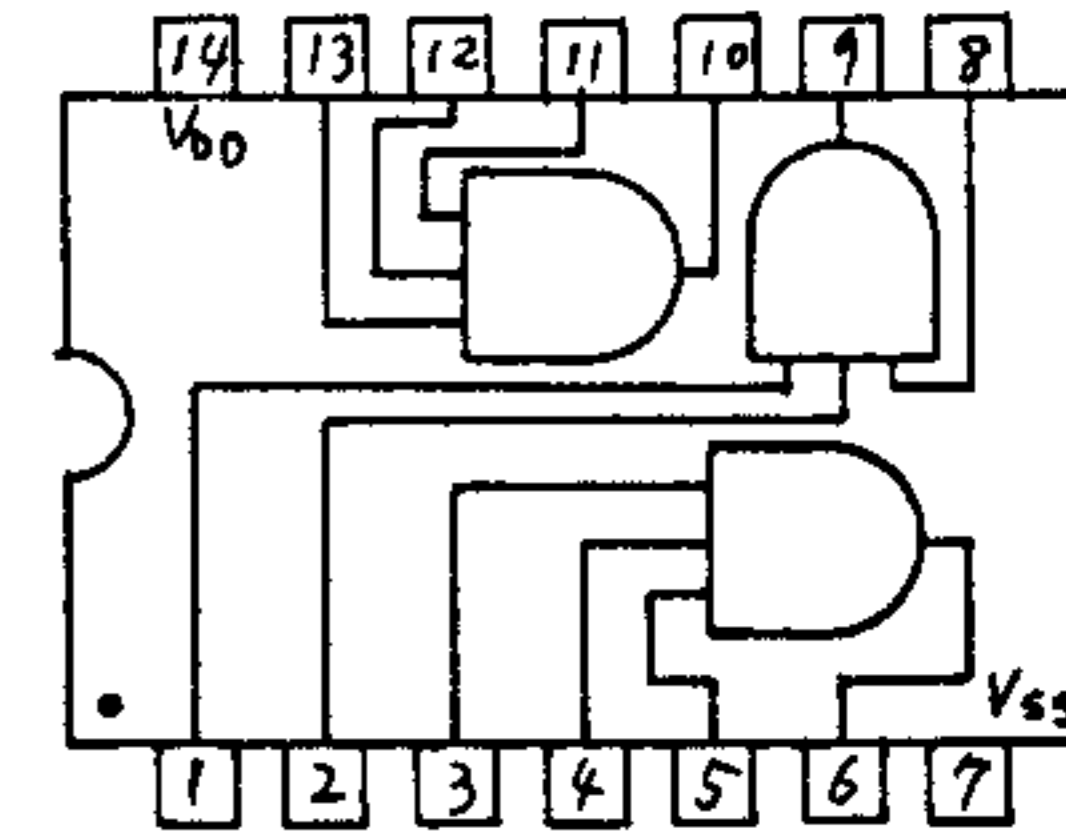
4070, 4030, 4507
4070は、4030を改良したもの



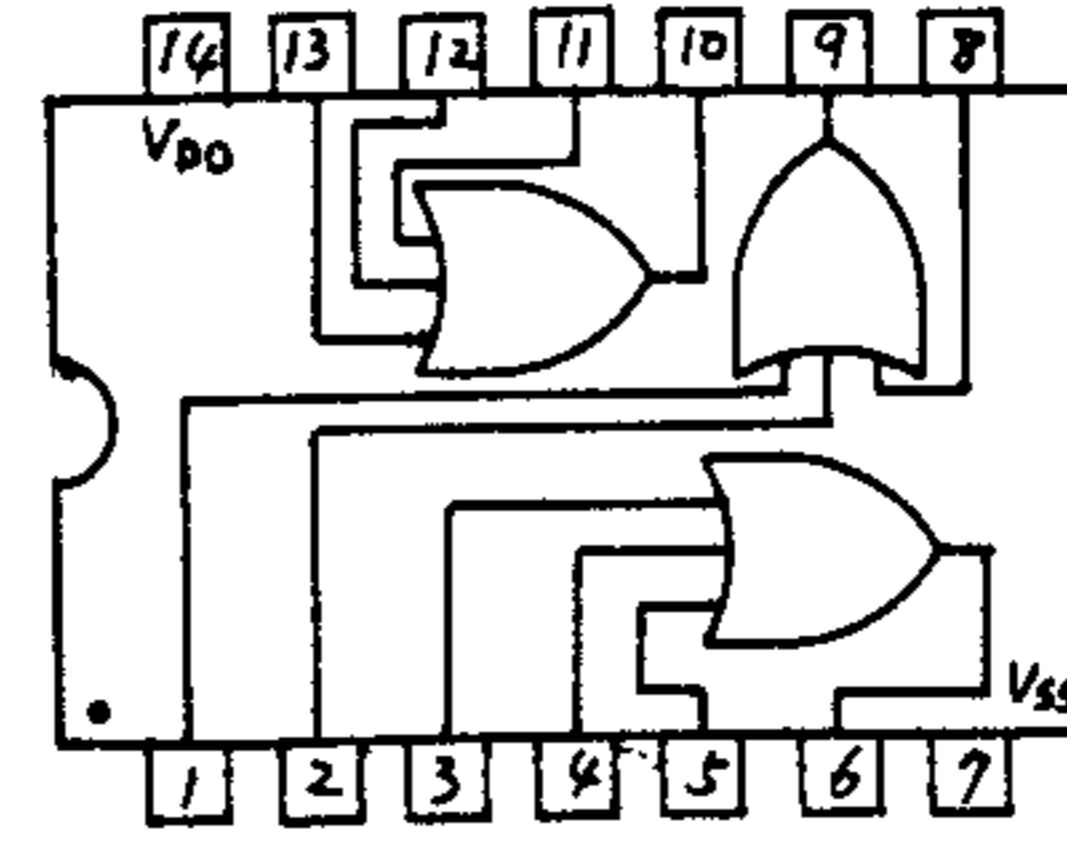
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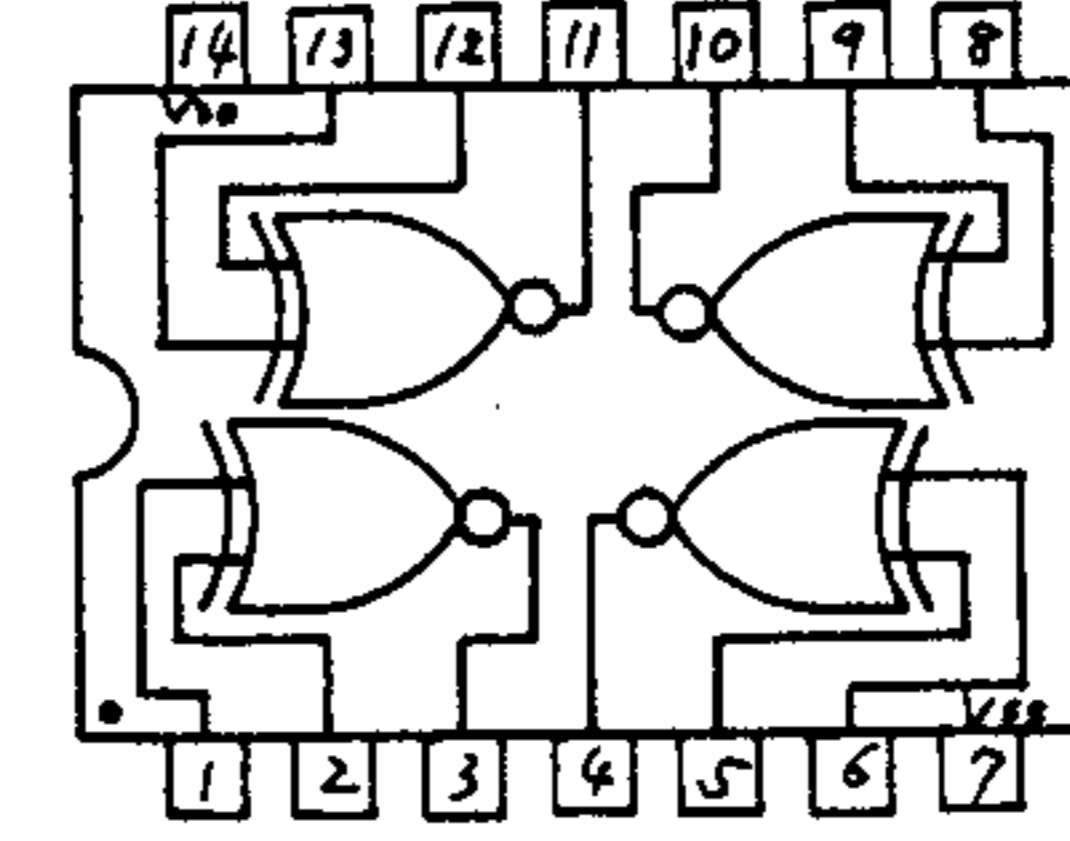
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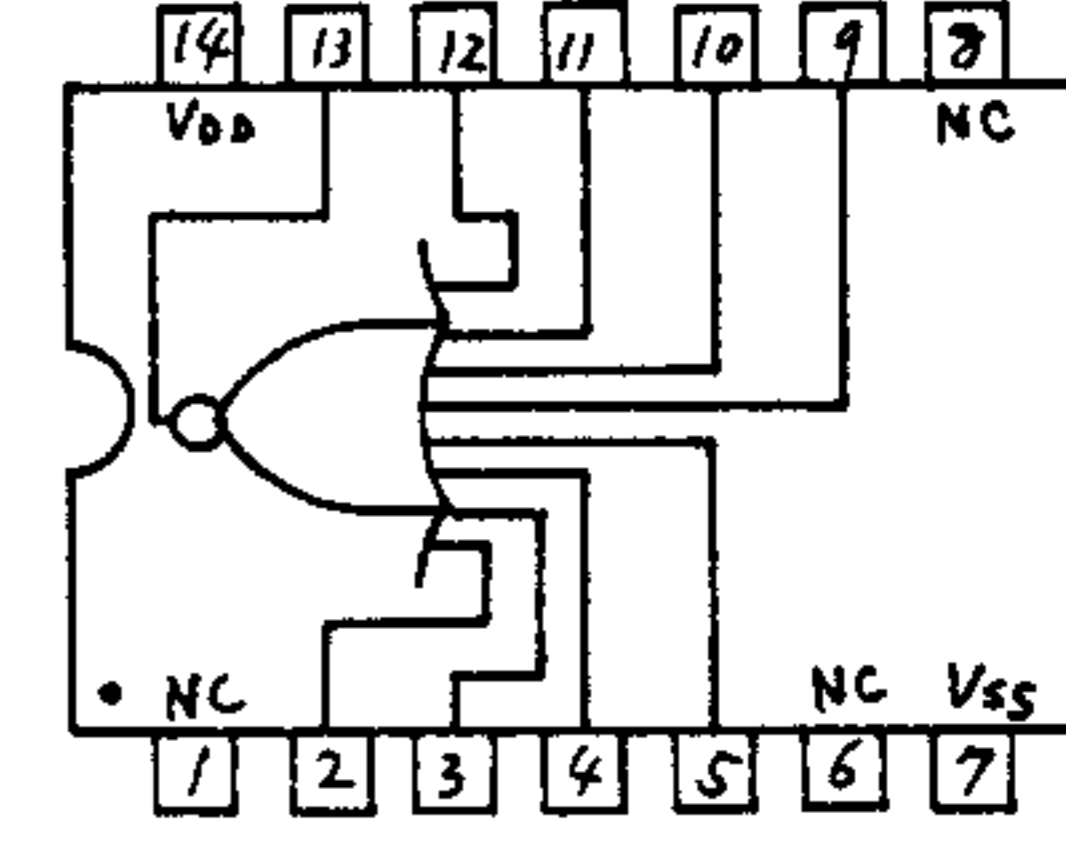
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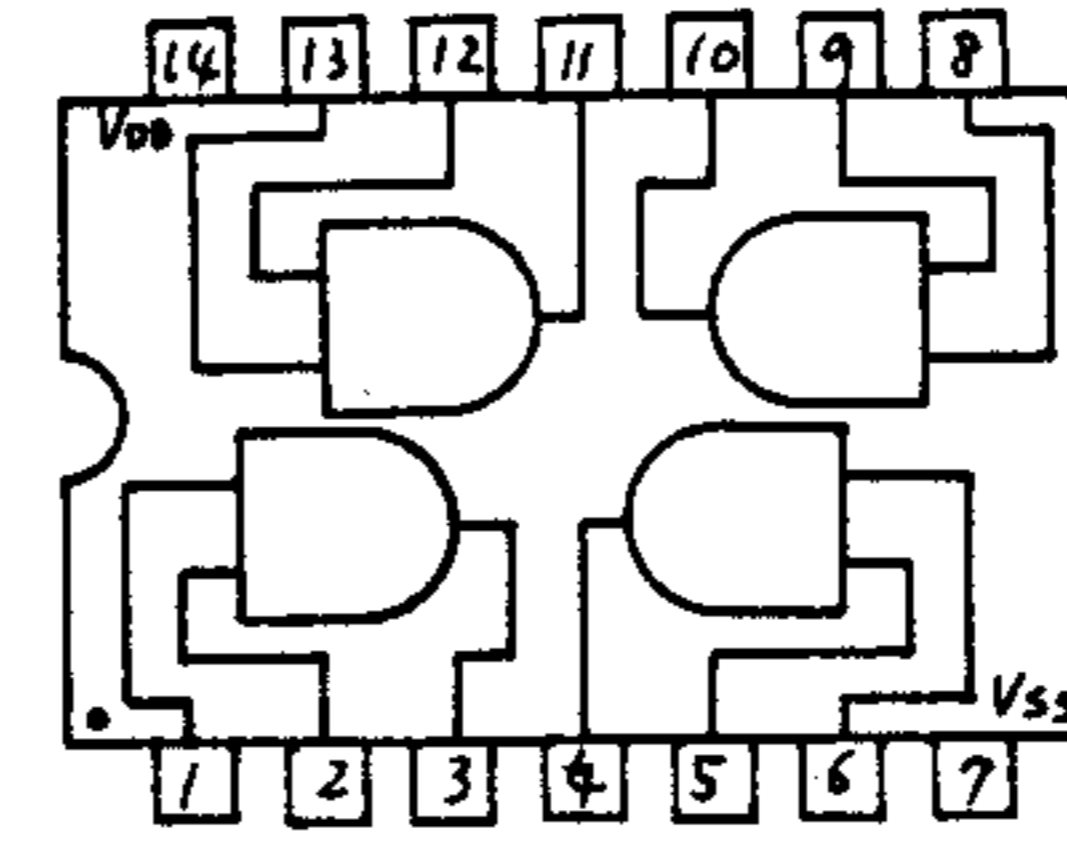
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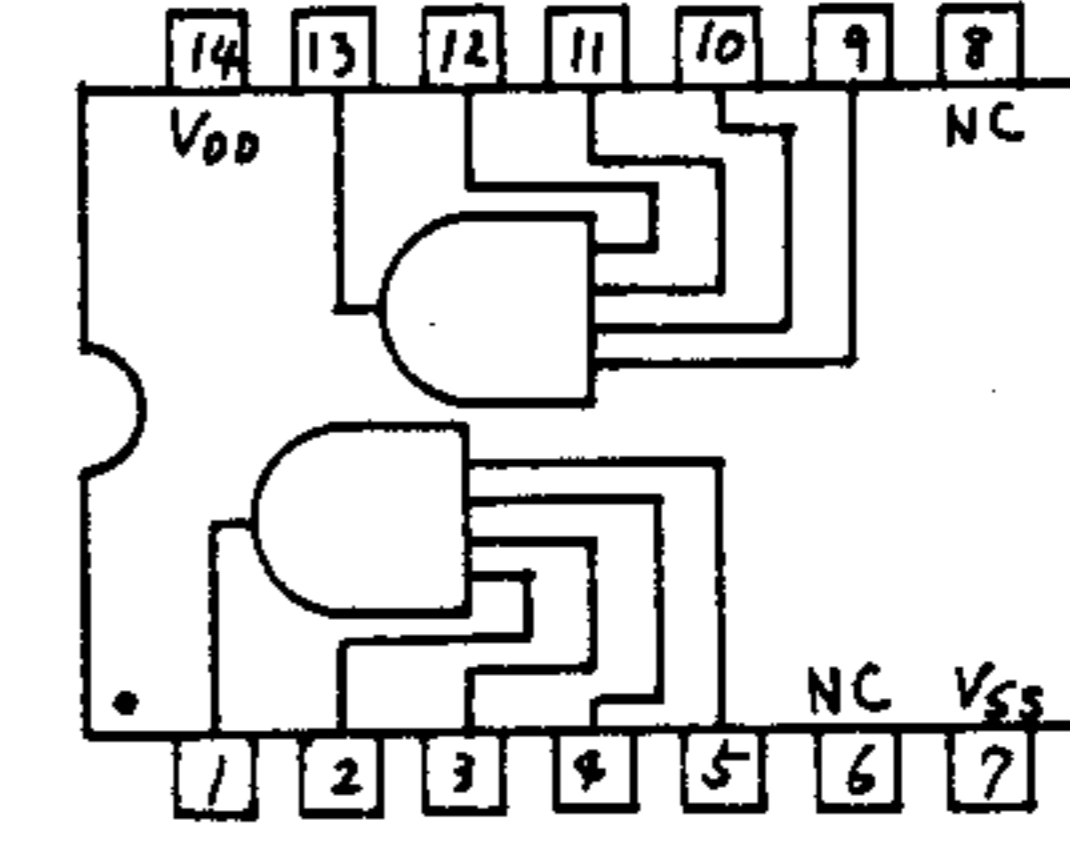
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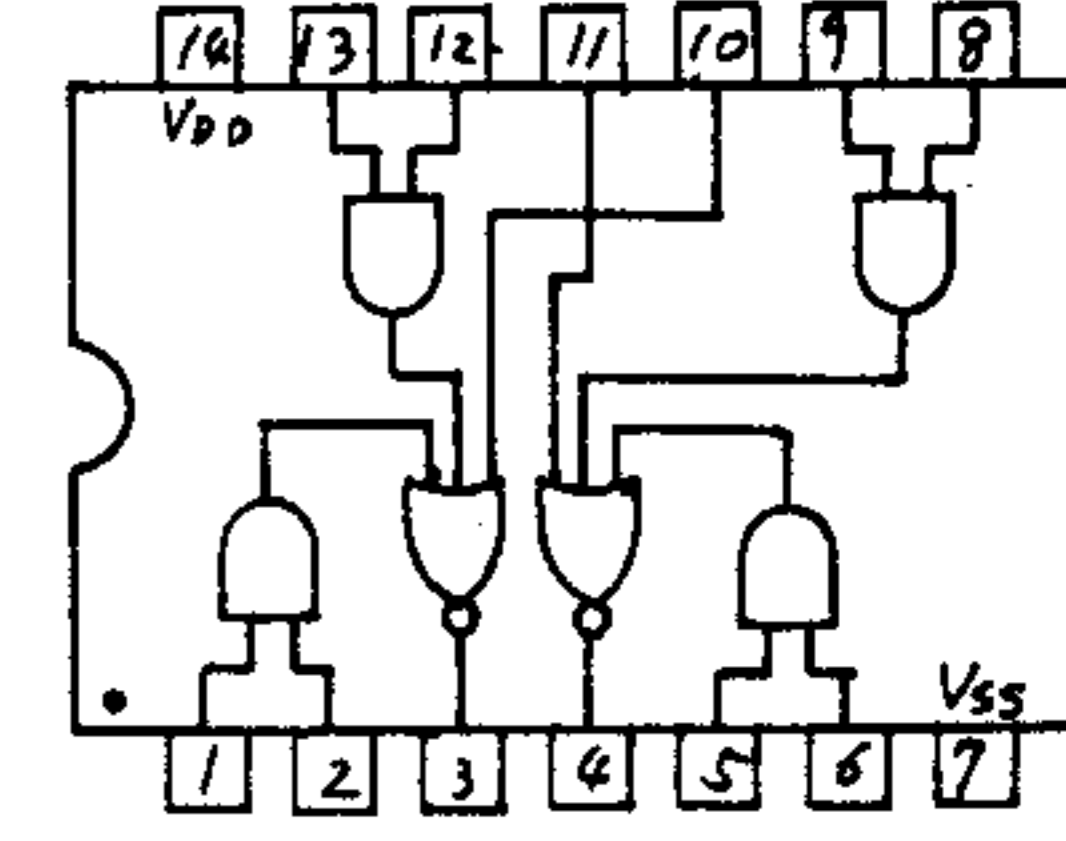
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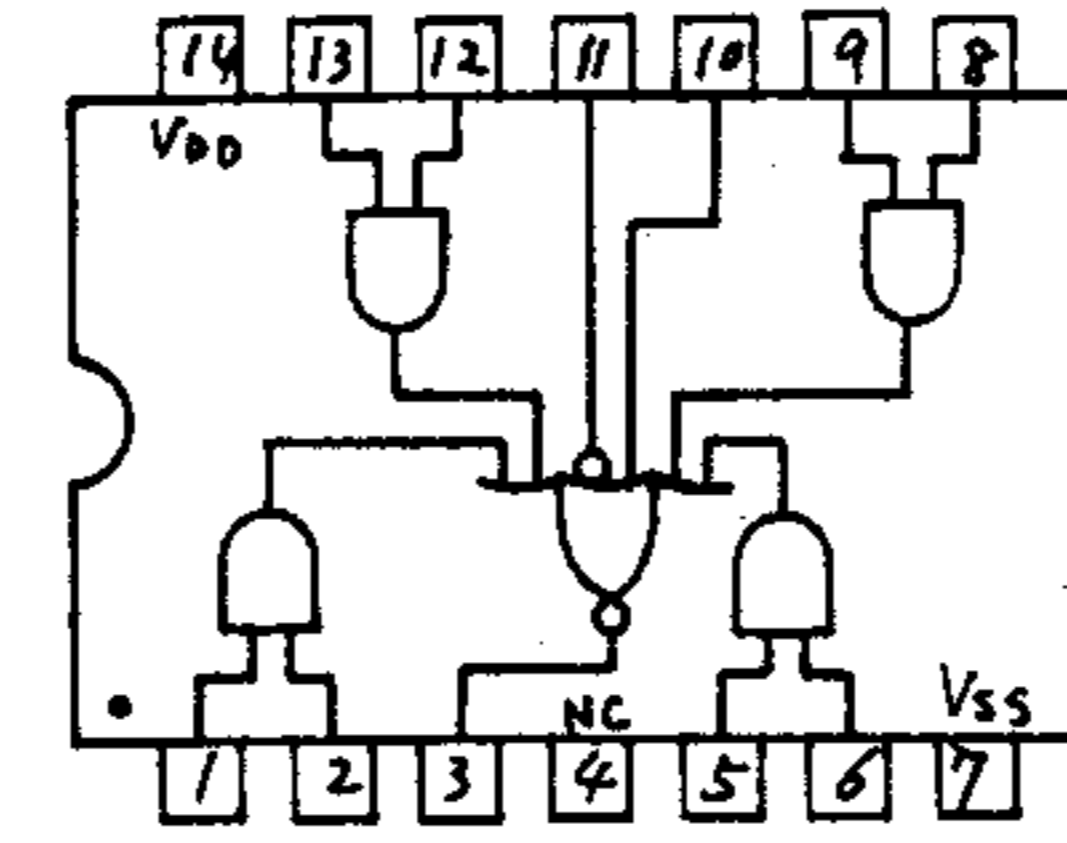
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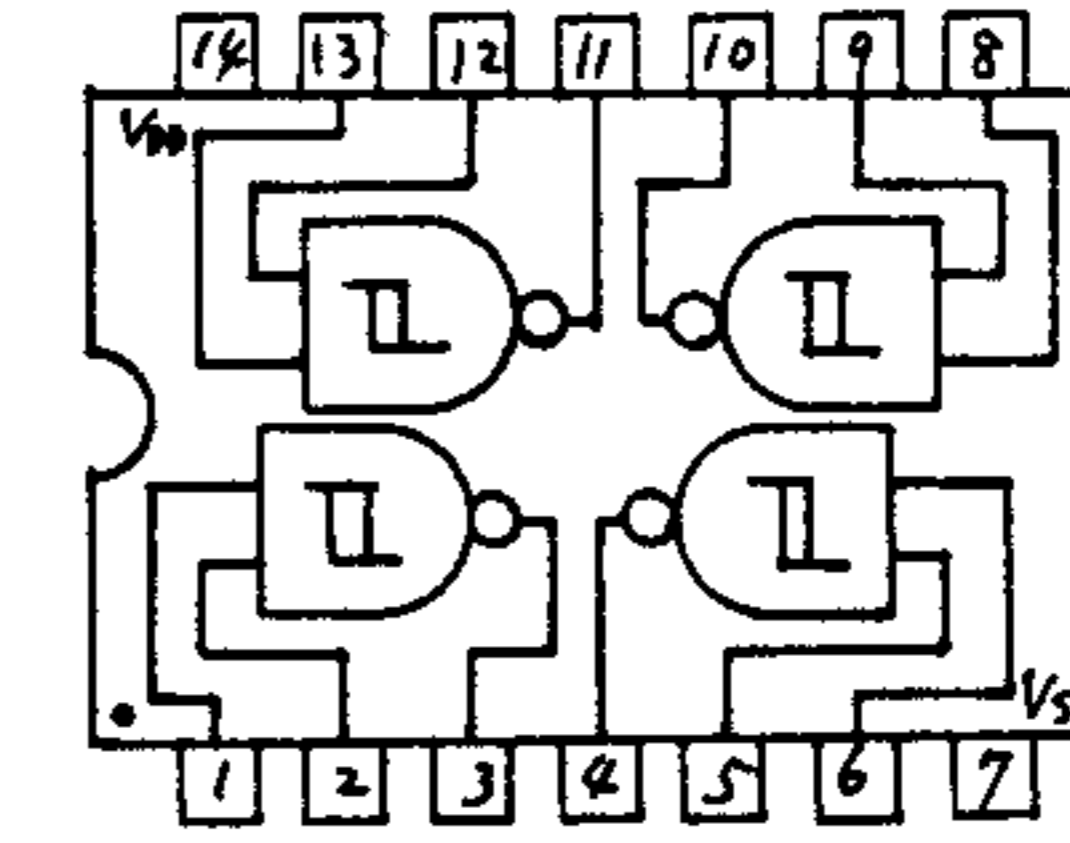
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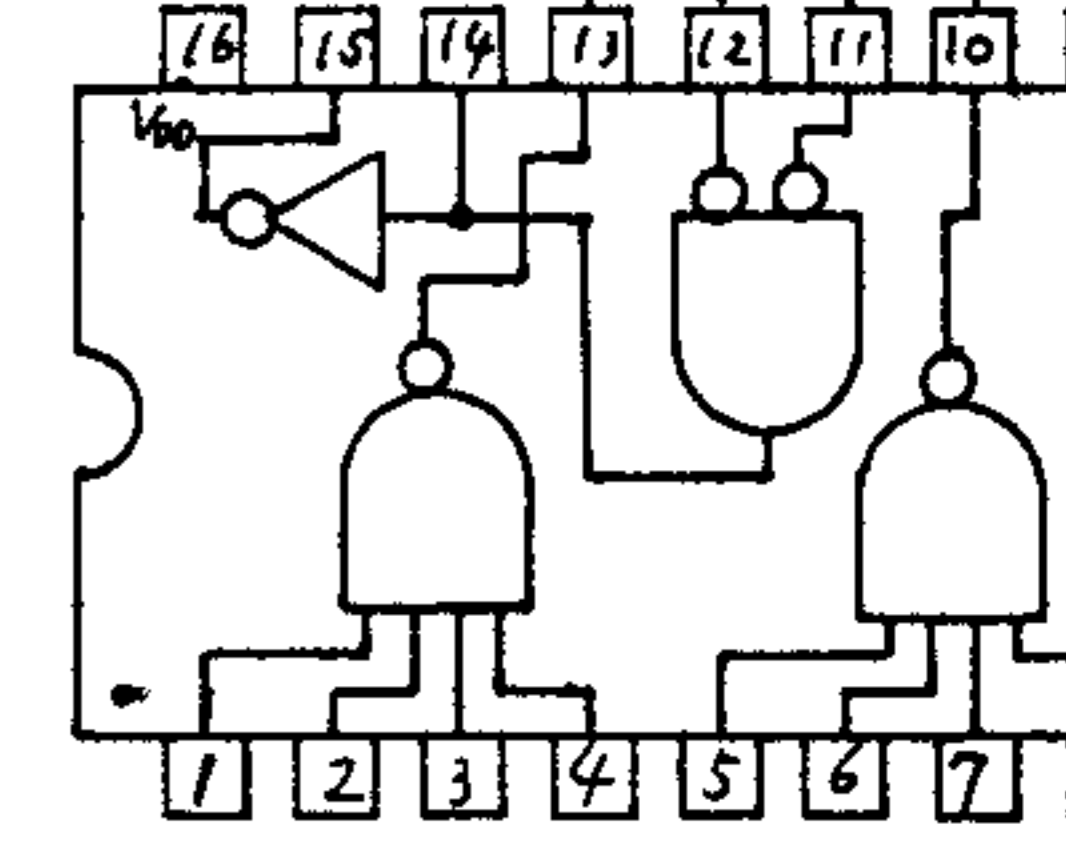
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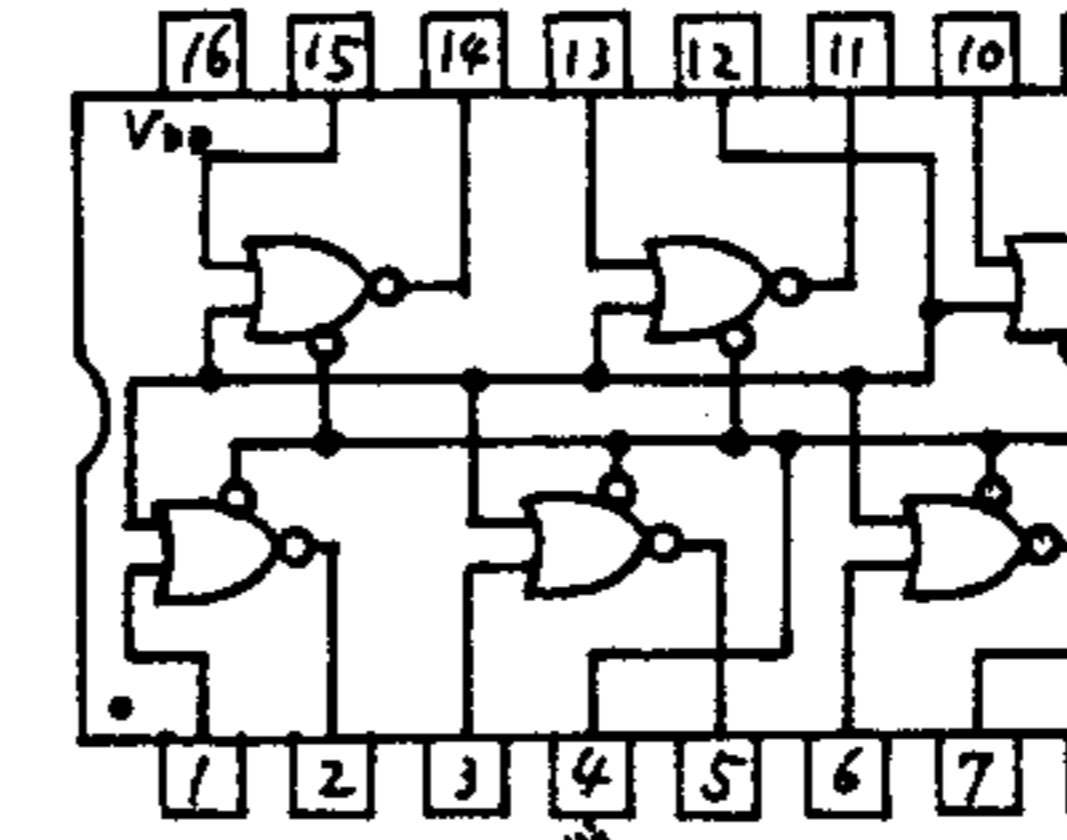
4086



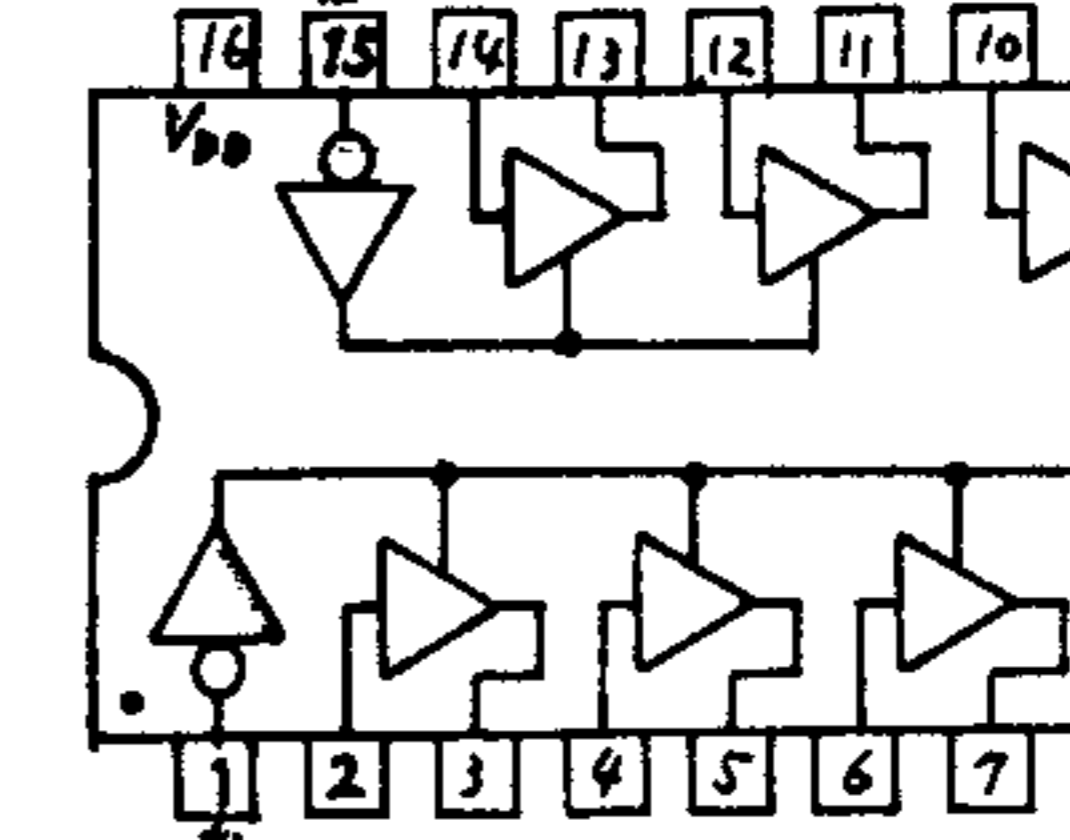
4093 NAND シュミットトリガ



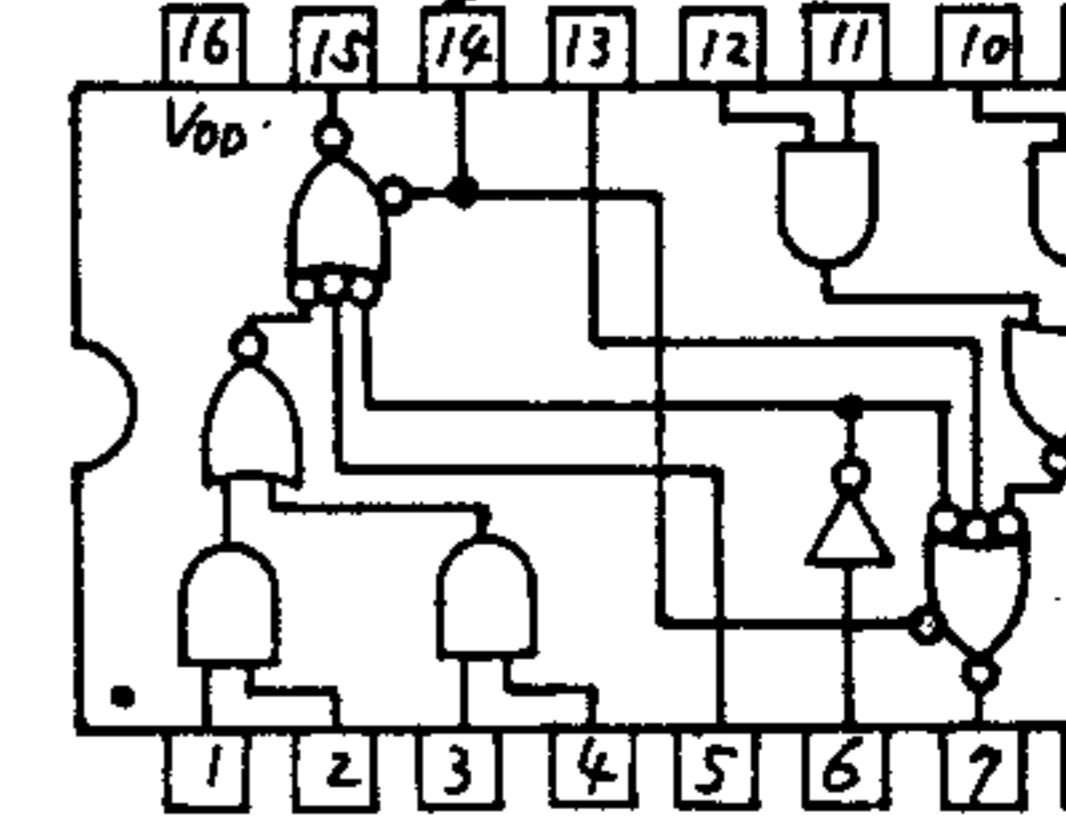
4501 8入のAND/NANDにもなる



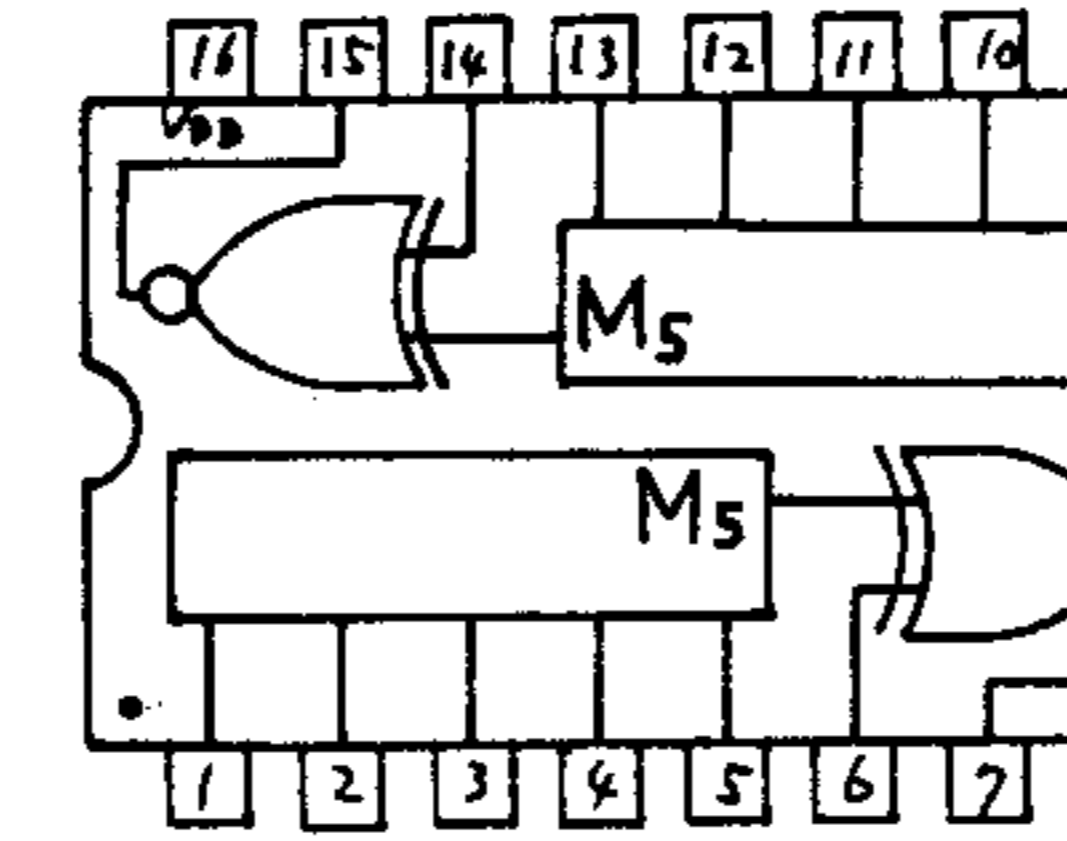
4502 * 1: High Z



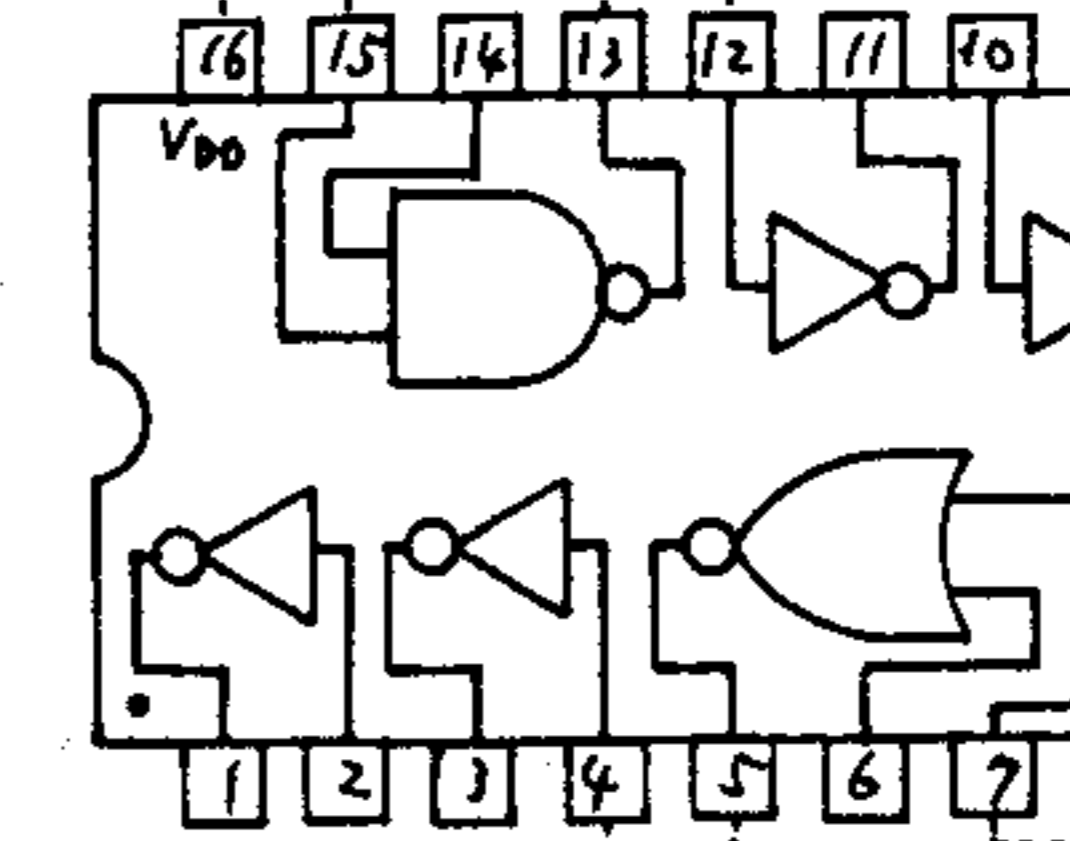
4503, 40097 * 1: High Z



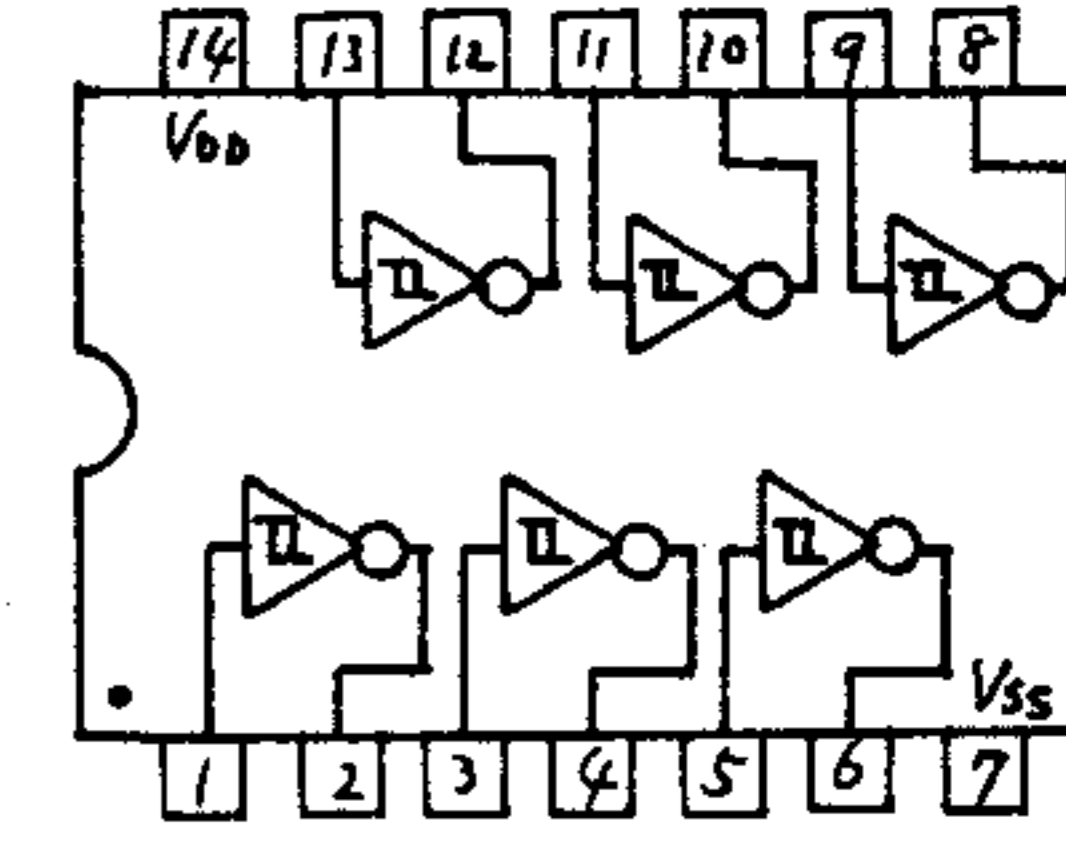
4506 * 1: High Z



4530 5入力多数決論理回路



4572 6INV, AND, OR



4584 シュミットトリガ